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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/726,618	12/01/2000	Hiroshi Ryu	OSP-9961	1537

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EXAMINER	
PALADINI, ALBERT WILLIAM	

ART UNIT	PAPER NUMBER
2125	

DATE MAILED: 05/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/726,618	RYU ET AL.	
	Examiner	Art Unit	
	Albert W Paladini	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The specification is objected to because it does not meet the objectives of the Manual of Patent Examining Procedure.

Under the BRIEF SUMMARY OF THE INVENTION from pages 4-6, the first eight aspects of the invention are enumerated. This enumeration consists of a verbatim statement of claims 1-8. The Manual of Patent Examining Procedure states in paragraph 608.01(g) that the specification or description is a dictionary of the claims. Specifically, the MPEP states, "The description is a dictionary for the claims and should provide clear support or antecedent basis for all terms used in the claims. See 37 CFR 1.75, MPEP § 608.01(i), § 608.01(o), and § 1302.01."

The claims are written in legal language to show the metes and bounds of the invention. The objective and content of the brief description as explained in the MPEP is

"37 CFR 1.73. Summary of the invention.

A brief summary of the invention indicating its nature and substance, which may include a statement of the object of the invention, should precede the detailed description. Such summary should, when set forth, be commensurate with the invention as claimed and any object recited should be that of the invention as claimed.

Since the purpose of the brief summary of invention is to apprise the public, and more especially those interested in the particular art to which the invention relates, of

the nature of the invention, the summary should be directed to the specific invention being claimed, in contradistinction to mere generalities which would be equally applicable to numerous preceding patents. That is, the subject matter of the invention should be described in one or more clear, concise sentences or paragraphs. Stereotyped general statements that would fit one case as well as another serve no useful purpose and may well be required to be cancelled as surplus usage, and, in the absence of any illuminating statement, replaced by statements that are directly in point as applicable exclusively to the case in hand.

The brief summary, if properly written to set out the exact nature, operation, and purpose of the invention, will be of material assistance in aiding ready understanding of the patent in future searches. ** The brief summary should be more than a mere statement of the objects of the invention, which statement is also permissible under 37 CFR 1.73.

The brief summary of invention should be consistent with the subject matter of the claims. Note final review of application and preparation for issue, MPEP § 1302."

Therefore the Brief Summary and the Description should be written so that a person of ordinary skill in the field will have a technical understanding of the objectives, methodology, functional operation, and elements of the invention. Since one of the objectives of the specification is to provide a dictionary of the claims, a verbatim statement of the claims does not meet this objective.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

3. Claims 1-8 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01.

Claim 1

Line 7 recites, "inheriting the circuit base classes prepared by the library." The term "inheriting" is passive and implies that one or more actions must be initiated elsewhere to cause the "circuit base classes" to be inherited or received. The steps, which initiate these actions, are missing.

Claim 10

Line 9 recites, "inheriting the circuit base classes prepared by the library." The term "inheriting" is passive and implies that one or more actions must be initiated elsewhere to cause the "circuit base classes" to be inherited or received. The steps, which initiate these actions, are missing.

Appropriate correction and clarification are required.

4. Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01.

Claim 9

Lines 7-9 recite "means accessing the storage means and describing the circuit modules to be simulated as classes by inheriting the circuit base classes stored in the library." The term "inheriting" is passive and implies that one or more elements must deliver or provide the "circuit base classes." These elements are missing.

Appropriate correction and clarification are required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malin (4,965,743).

Malin discloses a simulation modeling tool and method which uses an object based language as explained in column 12, lines 4-17 which state "FIG. 1, a diagram illustrating the use of the qualitative modeling tool loaded into a general purpose digital computer for creating, simulating, experimenting with and analyzing qualitative models. This qualitative modeling tool (or as stated above is often referred to as the "tool") built upon an object-oriented language (KEE.TM. by IntelliCorp) and a discrete event simulator (SimKit.TM. by IntelliCorp) with additional functionality provided by the underlying LISP programming environment (Symbolics) is the preferred embodiment of the invention. Even though this is the preferred embodiment, there is nothing about the invention that precludes it from being implemented in various manifestations other than the one described here." The application of the technique to circuits is described in column 3, lines 38-48 which state "Qualitative reasoning approaches typically lack explicit representations of time, duration, and delays, which are often used by a mental modeler, especially to analyze interacting dynamic processes. B. C. Williams, "Qualitative Analysis of MOS Circuits", Artificial Intelligence, December 1984, Vol. 24, discusses some of the limitations of these approaches, and presents a general approach to representing time qualitatively and reasoning about qualitative episodes for use in temporal constraint propagation, but not in discrete event simulation." The preparation of base classes describing modules a classes in a library is described in column 10, lines 20-36 which state "The library design module supports building library knowledge bases that contain component classes and elements pertinent to the particular domain of continuous activities, functions and behavior being modeled. The continuous behavior is defined discretely with respect to invocation statements, effect statements and time delays. All functionality of the components is defined in terms of variable cluster instances, independent processes and modes which are defined in terms of their mode transition processes and mode dependent processes. Library elements include components, processes, relation types and language elements, which, in turn, include value classes, operators and operations. Library elements are organized in hierarchical subclasses and are useful in defining models of both physical objects and abstract concepts, for example, as condition states associated with a medical diagnosis." Malin teaches combining the modules described in the classes in column 10, lines 37-47 which state "The model construction module supports building models by making component instances of the component classes and connecting them with appropriate relations. The simulation module supports the simulation of the models built by the model construction module without dependence on model configuration. The tool initializes models with predefined components by executing a specialized initialization routine and placing each component in the model in an event list. The model is run by executing events on the event list using a discrete event simulator until the list is empty."

Malin does not teach inheriting the circuit base classes which is a limitation of independent claims 1, 9, and 10. Since, as explained in paragraphs 2-4, the claims are incomplete because the steps and elements to perform inheriting are missing, the inheritance limitations are not addressed because they would not have been obvious to one of ordinary skill in the art.

Relevant Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Balakrishnan (6,135,647) discloses a system and method for representing a system level RTL hardware design using an HDL independent RTL representation and translation into synthesizable RTL code. The present invention creates an object-oriented library which can be used to implement RTL hardware designs in terms of HDL independent objects. Instead of implementing multiple HDL instances of hardware modules, the invention enables software tool programmers to implement one HDL-independent instance of the hardware module. As a result, a programmer can focus his efforts on generating the functionality of the module and can be relieved from the time consuming task of generating the detailed syntax of multiple HDLs. The present invention also maintains synchronization across multiple HDLs so that a software designer can generate HDL code for any supported HDL, e.g., Verilog or VHDL, thus making software maintenance easier.

Bargh (6,223,142) discloses a method and system that utilize the expressiveness of hardware description languages for incrementally compiling instrumentation logic into a simulation model of a digital circuit design. A simulation model that includes a design entity file of a digital circuit design is generated. Next, an instrumentation entity file is associated with the design entity file, thereby producing an instrumented design entity file. Finally, and during the process of compiling the simulation model, for the instrumented design entity file: searching for a consistent and previously compiled version of said instrumented design entity file. In response to finding a consistent and previously compiled version, loading the consistent and previously

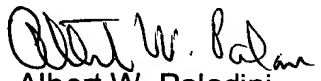
compiled version into the simulation model. In response to finding no consistent and previously compiled version, loading and compiling the instrumented design entity file.

Patterson discloses a placement system for simulation of a logic model where libraries of predeveloped blocks of logic have been developed that can be included in an FPGA design. Such library modules include, for example, adders, multipliers, filters, and other arithmetic and DSP functions from which complex designs can be readily constructed. The use of predeveloped logic blocks permits faster design cycles, by eliminating the redesign of duplicated circuits. Further, such blocks are typically well tested, thereby making it easier to develop a reliable complex design. Another embodiment of the invention is implemented in a high-level object-oriented programming language called Java.

9. Any inquiry concerning this communication or earlier communication from the examiner should be direct to Albert W. Paladini whose telephone number is (703) 308-2005. The examiner can normally be reached from 7:30 to 3:30 PM on Monday, Tuesday, Thursday, and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Leo P. Picard, can be reached on (703) 308-0538. The official fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



Albert W. Paladini
Primary Examiner
Art Unit 2125

May 10, 2004